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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/827,676	04/06/2001	Tsutomu Tanaka	09792909-4970	6747

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EXAMINER	
VU, QUANG D	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 07/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/827,676	TANAKA ET AL.	
	Examiner	Art Unit	
	Quang D Vu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *amendment filed on 03/04/2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *4-9,11 and 13* is/are pending in the application.

4a) Of the above claim(s) *14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *4-9,11 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 4-7, 9 and 11 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No. 6,281,552 to Kawasaki et al.

Kawasaki et al. (figures 1A-C, 2A-2C, 6) teach a method of making a bottom-gate thin-film transistor comprising:

forming a gate electrode (102) on a substrate (101);

forming a gate insulating film (105) on the gate electrode;

forming a laminate on the gate insulating film (105), comprising:

forming a precursor film (106) for an active layer, and

forming a protective spacer film (110) on the precursor film (106) without using an etching process, the protective spacer film (110) having a thickness of 100 nm or less (column 6, line 40);

implanting a dopant when forming a source-drain region (figure 1C) of the precursor film (106) for the active layer through the protective spacer film (110) without etching the protective spacer film (110); and

activating the implanted dopant so that a non-doped portion constitutes the active layer (figures 1B-2A; column 7, lines 45-55).

It is inherent that the protective spacer film is a protective insulating film because it protects the surface of the device.

Regarding claim 5, Kawasaki et al. teach the active layer comprises a crystallized silicon film. In thin film transistor (TFT), the crystallized silicon film is normally a polysilicon.

Regarding claim 6, Kawasaki et al. teach a method of making a TFT, wherein, in the laminate forming step, an amorphous silicon film is formed on the gate insulating film (105), the amorphous silicon film is crystallized to form a crystallize silicon film, and the protective spacer film (110) is formed on the crystallize silicon film (106) (column 5, line 62 – column 6, line 14).

Regarding claim 9, Kawasaki et al. disclose a heat treatment step is conducted to activate the impurity elements in the silicon film (column 7, lines 45-55). It is inherent that the heat treatment step would also recover the defects formed in the protective spacer film. Therefore, Kawasaki et al. inherently disclose the defects formed in the protective spacer film can be recovered after the heat treatment.

Regarding claim 11, Kawasaki et al. teach forming an interlayer insulating film (151), a transparent electrode (161), and an alignment layer (601) on a protective spacer film of the bottom gate thin film transistor to comprise a TFT substrate; and interposing a liquid crystal (605) between the TFT substrate and a counter substrate (602) provide with counter electrode (603) (see figure 6).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. in view of US Patent No. 6,063,654 to Ohtani.

The disclosures of Kawasaki et al. are discussed as applied to claims 4-7 above, Kawasaki et al. differ from the claimed invention by not showing to form the oxide layer on the amorphous silicon film through thermal oxidation. However, Ohtani (figures 3A-E) teaches to form the oxide layer on the amorphous silicon film (203) through thermal oxidation (column 9, lines 23-29). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Ohtani into the device taught by Kawasaki et al. because the oxide film through thermal oxidation improves wetting of the surface of the amorphous silicon film to suppress the solution from being repelled. The combined device shows that the protective spacer film is formed on a surface of the amorphous silicon film by surface oxidation of the amorphous silicon film, and then the amorphous silicon film is crystallized to form a crystallize silicon film.

5. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kawasaki et al. in view of US Patent No. 6,420,758 to Nakajima.

Regarding claim 13, Kawasaki et al. teach forming an interlayer insulating film (151) on a protective spacer of the bottom gate thin film transistor (see figure 2C). Kawasaki et al. differ from the claimed invention by not forming an organic EL element driven by the bottom gate thin film transistor on the interlayer insulating film. However, Nakajima teaches forming an organic EL element (3045) driven by the bottom gate thin film transistor on the interlayer insulating film (3042) (see figure 21; column 23, line 24 – column 25, line 62). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the teaching of Nakajima into the method taught by Kawasaki et al. because the organic EL element improves the quality of the image.

Response to Arguments

6. Applicant's arguments filed 03/04/2003 have been fully considered but they are not persuasive.

Applicant's main arguments include: (A). Kawasaki et al. do not teach or suggest a method of making a bottom-gate thin film transistor including the steps of: forming a laminate on the gate insulating film, comprising: forming a precursor film for an active layer, and forming a protective insulating film on the precursor film without using an etching process, the protective insulating film having a thickness of 100 nm or less; implanting a dopant when forming a source-drain region of the precursor film for the active layer through the protective insulating film without etching the protective spacer film; and activating the implanted dopant so that a non-doped portion constitutes the active layer; and (B) Kawasaki et al. do not teach or suggest the protective insulating film is formed on the precursor film without etching the protective

insulating film. Thereafter, the precursor film is implanted with a dopant through the protective insulating film without etching when forming the LDD region or the source-drain region.

With respect to applicant's Argument A, it is noted that Kawasaki et al. teach forming a laminate on the gate insulating film (105), comprising: forming a precursor film (106) for an active layer, and forming a protective spacer film (110) on the precursor film (106) without using an etching process, the protective spacer film (110) having a thickness of 100 nm or less (column 6, line 40); implanting a dopant when forming a source-drain region (figure 1C) of the precursor film (106) for the active layer through the protective spacer film (110) without etching the protective spacer film (110); and activating the implanted dopant so that a non-doped portion constitutes the active layer (figures 1B-2A; column 7, lines 45-55). It is inherent that the protective spacer film is a protective insulating film because it protects the surface of the device.

With respect to applicant's Argument B, it is noted that Kawasaki et al. teach the protective spacer film (110) is formed on the precursor film (106) without etching the protective spacer film (110). Thereafter, the precursor film (106) is implanted with a dopant through the protective spacer film (110) without etching the protective spacer film (110) when forming the source-drain region (figure 1C).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
July 11, 2003

Thomas
TC — 2800
7-11-03